AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising:

opening a window for helium implantation on a hydride vapor phase epitaxy (HVPE) grown n^+ GaN quasi-substrate layer, using optical lithography;

implanting helium on the n+ GaN quasi-substrate layer over the window for helium implantation, so as to provide an insulating layer for contact pads of the device;

opening a window for collector fingers using E-beam lithography;

depositing an ohmic metallization layer over the window for the collector fingers;

lifting-off ohmic metallization, thereby forming the collector fingers;

opening a window for a self-aligned base recess using optical lithography; ~~and~~

etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage; [[.]]

opening a window for a collector contact pad, using optical lithography;

depositing a high quality silicon nitride layer over the window for a collector contact pad; and

lifting-off or wet chemical etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

Claim 2 (Canceled):

Claim 3 (Currently Amended): The method of claim [[2]] 1 wherein the high quality silicon nitride layer is about 1000-2000Å thick, and is deposited over the window for helium implantation via plasma enhanced chemical vapor deposition (PECVD).

Claim 4 (Currently Amended): The method of claim [[2]] 1 further comprising:

opening a window for Ti metallization of the collector contact pad using optical lithography;

depositing Ti over the window for Ti metallization of the collector contact pad; and

lifting-off Ti metallization, thereby forming a Ti collector contact pad.

Claim 5 (Original): The method of claim 4 further comprising:

opening a window for a second Ti metallization of the collector contact pad using optical lithography;

depositing Ti over the window for the second Ti metallization of the collector contact pad; and

lifting-off second Ti metallization, thereby forming a Ti cap over the collector contact pad.

Claim 6 (Currently Amended): The method of claim [[2]] 1 wherein depositing Ti over the window for Ti metallization of the collector contact pad includes depositing Ti/Au at thicknesses of about 500Å/1000Å, respectively, using e-beam evaporation.

Claim 7 (Canceled).

Claim 8 (Currently Amended): The method of claim ~~7~~ 22 wherein an anneal is performed post-base metallization so as to provide the base contact pad with low reverse current leakage and low contact resistance.

Claim 9 (Original): The method of claim 1 further comprising:

opening an emitter etch/contact window using optical lithography;

etching an emitter recess to the n^+ GaN quasi-substrate layer;

depositing an emitter ohmic metallization layer over the etched emitter recess; and

lifting-off emitter ohmic metallization, thereby forming an emitter contact pad.

Claim 10 (Original): The method of claim 1 wherein the emitter ohmic metallization layer includes at least one of titanium, aluminum, nickel, and gold.

Claim 11 (Canceled).

Claim 12 (Original): The method of claim 1 wherein the helium implantation is achieved with an implant depth of about 2 μm.

Claim 13 (Original): The method of claim 1 wherein the ohmic metallization layer over the window for the collector fingers is Ti/Ni with thicknesses of 100Å and 400Å, respectively.

Claim 14 (Original): The method of claim 1 wherein the device has a plurality of collector fingers about 0.2 μm wide and having a finger pitch between 1:1 and 1:3.

Claims 15 -20 (Canceled)

Claim 21 (Currently Amended): A method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising:

opening a window for a base recess; and

etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage[[.]]

opening a window for RF test pad metallization using optical lithography;

depositing an RF test pad metallization layer; and

lifting-off RF test pad metallization, thereby providing RF test pads.

Claim 22 (New): A method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising:

opening a window for helium implantation on a hydride vapor phase epitaxy (HVPE) grown n^+ GaN quasi-substrate layer, using optical lithography;

implanting helium on the n+ GaN quasi-substrate layer over the window for helium implantation, so as to provide an insulating layer for contact pads of the device;

opening a window for collector fingers using E-beam lithography;

depositing an ohmic metallization layer over the window for the collector fingers;

lifting-off ohmic metallization, thereby forming the collector fingers;

opening a window for a self-aligned base recess using optical lithography;

etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage; depositing conformal silicon nitride for passivation of the recessed base layer;

directionally etching to remove silicon nitride on planes parallel to the n^+ GaN quasi-substrate layer;

depositing a base metallization layer; and

lifting-off base metallization, thereby forming a base contact pad.

Claim 23 (New): The method of claim 22 wherein the emitter ohmic metallization layer includes at least one of titanium, aluminum, nickel, and gold.

Claim 24 (New): The method of claim 22 wherein the helium implantation is achieved with an implant depth of about 2 μm.

Claim 25 (New): The method of claim 22 wherein the ohmic metallization layer over the window for the collector fingers is Ti/Ni with thicknesses of 100Å and 400Å, respectively.

Claim 26 (New): The method of claim 22 wherein the device has a plurality of collector fingers about 0.2 μm wide and having a finger pitch between 1:1 and 1:3.